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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/573,495	03/24/2006	Kazumi Naito	Q77806	9323

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EXAMINER	
CRAWFORD, LATANYA N	
ART UNIT	PAPER NUMBER
2813	

NOTIFICATION DATE	DELIVERY MODE
09/30/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/573,495	NAITO, KAZUMI	
	Examiner	Art Unit	
	LATANYA CRAWFORD	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *1-4 and 22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-21,23 and 25-27* is/are rejected.

7)☒ Claim(s) *24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2010* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the correspondence filed on 7/08/2010.

currently, claims 1-27 are pending

Response to Arguments

2. Applicant's arguments filed 7/08/2010 have been fully considered but they are not persuasive.

3. Applicant argues: "Yoshida et al does not disclose forming discrete fine protrusions having a specified dimension on a part of but less than the entire surface of the dielectric layer before energization as required by claims 20 and 21."

Examiner notes that Fig.2 of Yoshida et al shows a exploded view of the micropores in anode conductor 1 where polymer film 301 depict fine protrusions on dielectric layer 2. Although, polymer layer 301 is formed by electrolytic oxidative polymerization, a second conductive polymer (302) film is formed by electrolytic polymerization [0040] in view of fig.2, therefore the fine protrusions of formed by film 301 were formed prior to energization of a second energization of polymer film 302. Furthermore, the Examiner notes that the transitional term "comprising", which is synonymous with "including," "containing," or "characterized by," is inclusive or open-ended and does not exclude additional, unrecited elements or method steps. See, e.g., > Mars Inc. v. H.J. Heinz Co., 377 F.3d 1369, 1376, 71 USPQ2d 1837, 1843 (Fed. Cir. 2004). A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & Associates, Inc. v. Garlock,

Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984)

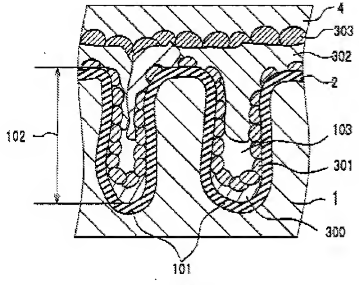


FIG. 2

4. Applicant argues: Consequently, the fine protrusions of the present invention and the conductive film 300 of Yoshida et al must be formed in shapes different from each other, and therefore fine protrusions having the claimed dimensions are not inherent in the method of Yoshida et al.

Examiner notes that in fig.2 conductive film 301 forms fine protrusions on a dielectric layer 2. The claim does not require that the conductive film be formed of shapes different from each other.

5. The semiconductor layer of claims 20 and 21 is made by energization *using the electric conductor as an anode*. That is, the present invention employs an electrolytic polymerization method using internal electrodes, which enables the present invention to attain the effects described at page 14, lines 20-27 of the specification. Yoshida et al, using *external* electrodes, has no disclosure from which one skilled in the art could foresee and realize the effects of the invention by employing internal electrodes.

Yoshida discloses the semiconductor layer (302) fig. 2 of claims 20 and 21 is made by energization using the electric conductor as an anode. The electric

conductor is used as an anode and is described by the Yoshida et al. in [0039][0052][0059]. Yoshida refers to element (1) [0039][0059] and element (10) [0052] as anode conductors. After the anode conductor undergoes chemical oxidative polymerization [0060], the anode conductor comprising an electrolytic layer and conductive polymer are further exposed to an electrolytic polymerization in which energization occurs [0061-0062]. In an interview conducted on 7/20/2010, applicant further provided explanation as to why the present invention is different from Yoshida and further stated *that a direct current of 20mA was passed for thirty minutes between the lead wire and a negative tantalum electrode plate disposed in the electrolytic solution as disclosed in [0083] of Applicant's published application.* Examiner notes that the claim does not require this limitation, only that the semiconductor layer is made by energization using the electric conductor as an anode which is taught by Yoshida. There is nothing in the claim to distinguish the anode (1) of Yoshida and the anode of the present invention.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 5-21, 23, 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida (US 2003/0133256 A1).

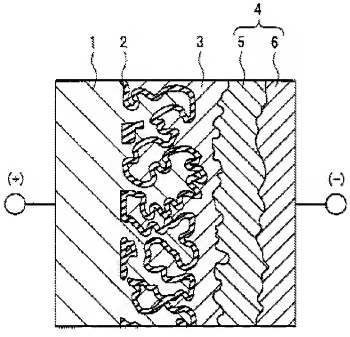


FIG. 1

Regarding claim 20, Yoshida et al. discloses a method for producing a capacitor comprising, as one electrode (1), an electric conductor having formed on the surface thereof a dielectric layer (2)and, as the other part electrode, a semiconductor layer (3) [0038] formed on the electric conductor by energization using the electric conductor as a anode [0035], wherein discrete feather-shaped fine protrusions are formed on a part of but less than the entire surface of the dielectric layer (in view of fig.1)before energization [0056][0072-0074] but is silent to having a width of about 0.1 to about 120 nm and a height of about 0.1 to about 600 nm. It would have been obvious to one of ordinary skill in the art at the time the invention was made that a width of about 0.1 to about 120 nm and a height of about 0.1 to about 600 nm would result since Yoshida et

al. teaches substantially identical structures (in view of recently submitted drawings fig. 5 compared to Yoshida et al. fig. 1), and substantially identical processes, a prima facie case of obviousness has been established. In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977).

Regarding claim 21, Yoshida et al. discloses a method for producing a capacitor comprising, as one electrode, an electric conductor (1) having formed on the surface thereof a dielectric layer (2) and, as the other part electrode, a semiconductor layer (3) [0038] formed on the electric conductor by energization using the electric conductor as the anode [0035], wherein discrete fine protrusions are formed on a part of but less than the entire surface of the dielectric layer (view fig. 1) before energization [0056][0072-0074], said electric conductor having inner pores formed therein, and wherein a majority of the fine protrusions overlay an outer surface of the dielectric layer fig. 1 but fails to teach having a width of 0.1to 60 nm. It would have been obvious to one of ordinary skill in the art at the time the invention was made that having a width of 0.1to 60 nm would result since Yoshida et al. teaches substantially identical structures (in view of recently submitted drawings fig. 5 compared to Yoshida et al. fig. 1), and substantially identical processes, a prima facie case of obviousness has been established. In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977).

Regarding claim 5, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 20 or 21, wherein the fine protrusion at least one member selected from a metal oxide [0059].

Regarding claim 6, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 20 or 21, wherein the electric conductor is at least one member selected from a metal [0059].

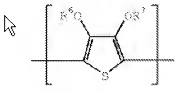
Regarding claim 7, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 20 or 21, wherein the electric conductor (1) is a laminated body having, as the surface layer, at least one member selected from an organic semiconductor and carbon (5/6) [0049] fig. 1

Regarding claim 8, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 20 or 21, wherein the dielectric layer mainly comprises at least one member selected from metal oxides such as Ta_2O_5[0059]

Regarding claim 9, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 20 or 21, wherein the semiconductor layer (3) is at least one member selected from an organic semiconductor layer and inorganic semiconductor [0038].

Regarding claim 10, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 9, wherein the organic semiconductor is at least one member selected from an organic semiconductor comprising an organic semiconductor mainly comprising tetracyano-quinodimethane [0038]

Regarding claim 11, Yoshida et al. discloses The method for producing a capacitor as claimed in claim 10, wherein the electrically conducting polymer containing a repeating unit represented by formula (1) is an electrically conducting polymer containing a structure unit represented by the following formula (3) as a repeating unit:



(3)

wherein R6 and R7 each independently represents a hydrogen atom, a linear or branched, saturated or unsaturated alkyl group having from 1 to 6 carbon atoms, or a substituent for forming at least one 5-, 6- or 7-membered saturated hydrocarbon cyclic structure containing two oxygen atoms when the alkyl groups are combined with each other at an arbitrary position, and the cyclic structure includes a structure having a vinylene bond which may be substituted, and a phenylene structure which may be substituted [0004].

Regarding claim 12, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 10, wherein the electrically conducting polymer is selected from polypyrrole [0004].

Regarding claim 13, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 11, wherein the electrically conducting polymer is poly(3,4-ethylenedioxythiophene) [0004].

Regarding claim 14, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 9, wherein the inorganic semiconductor is at least one compound selected manganese dioxide [0038].

Regarding claim 15, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 9, wherein the electrical conductivity of the semiconductor is from 10^{-2} to 10^{3} S/cm [0004][0038].

Regarding claim 16, Yoshida et al. discloses a capacitor produced by the production method claimed in claim 20 or 21 (in view of fig. 1).

Regarding claim 17, Yoshida et al teaches a capacitor produced as in claim 16 but is silent to the impregnation ratio of the semiconductor is 85% or more. It would have been obvious to one of ordinary skill in the art at the time the invention was made that the impregnation ratio of the semiconductor is 85% or more would result since Yoshida et al. teaches substantially identical structures (in view of recently submitted drawings fig. 5 compared to Yoshida et al. fig. 1), and substantially identical processes (in view of rejection for claim 20 and 21) a prima facie case of obviousness has been established. In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977).

Regarding claim 18, Yoshida et al. discloses an electronic circuit using the capacitor claimed in claim 16 (in view of fig. 1) [0002].

Regarding claim 19, Yoshida et al. discloses an electronic device using the capacitor claimed in claim 16 (in view of fig. 1)[0002].

Regarding claim 23, Yoshida et al. discloses a capacitor produced as in claim 21 but is silent to wherein 80% or more of the fine protrusions overlay an outer surface of the dielectric layer. It would have been obvious to one of ordinary skill in the art at the

time the invention was made that 80% or more of the fine protrusions overlay an outer surface of the dielectric layer would result since Yoshida et al. teaches substantially identical structures (in view of recently submitted drawings fig. 5 compared to Yoshida et al. fig. 1), and substantially identical processes (in view of rejection for 21) a prima facie case of obviousness has been established. In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977).

Regarding claim 25, Yoshida et al the method for producing a capacitor as claimed in claim 20 or 21, which comprises electrolytically forming the fine protrusions on the dielectric layer (2) [0036] in view of fig. 1.

Regarding claim 26, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 20, wherein the discrete feather-shaped fine protrusions (in view of fig. 1) but is silent to having a width of about 0.1 to about 60 nm and a height of about 0.1 to about 120 nm. It would have been obvious to one of ordinary skill in the art at the time the invention was made that a width of about 0.1 to about 60 nm and a height of about 0.1 to about 120 nm would result since Yoshida et al. teaches substantially identical structures (in view of recently submitted drawings fig. 5 compared to Yoshida et al. fig. 1), and substantially identical processes (in view of rejection for claim 20) a prima facie case of obviousness has been established. In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977).

Regarding claim 27, Yoshida et al. discloses the method for producing a capacitor as claimed in claim 21, wherein the discrete fine protrusions (in view of fig. 1)

but is silent to having a width of 0.1 to 30 nm. It would have been obvious to one of ordinary skill in the art at the time the invention was made that a width of 0.1 to 30 nm would result since Yoshida et al. teaches substantially identical structures (in view of recently submitted drawings fig. 5 compared to Yoshida et al. fig. 1), and substantially identical processes (in view of rejection for claim 21) a prima facie case of obviousness has been established. In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977).

Allowable Subject Matter

8. Claim 24 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LATANYA CRAWFORD whose telephone number is (571)270-3208. The examiner can normally be reached on Monday-Friday 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Landau can be reached on (571)-272-1731. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matthew C. Landau/
Supervisory Patent Examiner, Art Unit 2813

/LaTanya Crawford/
Examiner, Art Unit 2813